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10/677,830	10/02/2003	Bin Yang	CS02-090	9779

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EXAMINER	
YEVSIKOV, VICTOR V	
ART UNIT	**PAPER NUMBER**
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/677,830	Applicant(s) YANG ET AL.	
	Examiner Victor V Yevsikov	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/2/3*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al. (6,387,750 B1) in view of Dirnecker et al. (6,646,323 B2).

With respect to claim 1 Lai teaches a method of fabrication of a MIM capacitor comprising the steps of :

a) providing a semiconductor structure 200 having a first region and a capacitor region

b) forming a first conductive layer 202 over the semiconductor structure;

c) patterning the first conductive layer 202 to form a plurality of trenches in the capacitor region;

d) forming a capacitor dielectric layer 206 over the first conductive layer 202;

e) forming a top plate 208 over the capacitor dielectric layer in the capacitor region;

f) patterning the first conductive layer 202 in the first region to form first conductive patterns and a bottom plate.

Reference: figs. 2A-2E with corresponding text.

Lai teaches the features detailed previously but lacks a discussion on the method for forming an interlevel dielectric layer over the first conductive layer.

However, Dirnecker teaches the method for forming an interlevel dielectric layer 930 over the first conductive layer 910 (fig. 37 with corresponding text).

Therefore, it would have been obvious to one of ordinary skill in the art to forming an interlevel dielectric layer over the first conductive layer as taught by Lai/ Dirnecker as a means to insulate between the metal layers.

Claims 2 - 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Dirnecker.

With respect to claims 5,7 and 9 Lai teaches a method wherein:

5. the first conductive layer is comprised of Al, Cu and alloys of Al or Cu; and has a thickness in the range of between 6,000 and 10,000 Å (col.3, lns. 31-32).

7. the trenches extend down into the conductive layer between 24% and 84% of the thickness of the first conductive layer (col.3, lns. 35-37).

9. the capacitor dielectric layer has a thickness between 100 and 1000 Å and is comprised of a material selected from the group consisting of silicon oxide, silicon nitride (col.3, lns. 43-46).

With respect to claims 2- 4, 6, 8 and 10-12 Dirnecker teaches a method wherein:

2. further includes forming interconnects to electrically contact the top plate 450, the bottom plate 402 and the first conductive patterns 418 (figs. 25 and 26 with corresponding text).

3. the first conductive pattern comprise a n-l level wiring layer;

forming via contacts 920 in the interlevel dielectric layer 930 to contact the top plate 720, the bottom plate 910 and the first conductive patterns 910;

forming a second conductive line contacting the via contacts (fig. 37).

4. forming via contacts in the interlevel dielectric layer to contact the top plate, the bottom plate and the first conductive patterns;

forming second conductive layer contacting the via contacts, the second conductive layer is a n level metal layer; the first conductive patterns comprise a n-l level metal layer (fig. 37).

6. the plurality of trenches formed in a pattern of rows and columns (figs 28 and 29).

8. step (c) further comprises:

forming a trench resist layer over the first conductive layer;

the trench resist layer has openings that define areas where trenches will be formed in first conductive layer in the capacitor area;

patterning the first conductive layer to form a plurality of trenches in the capacitor region;

removing the trench resist layer (col.8, lines 34-52).

10 the top plate is formed by forming a top plate layer over the capacitor dielectric layer; and masking and patterning the top plate layer (fig.25).

11. step (f) comprises:

forming a bottom metal resist mask over the first conductive layer; the bottom metal resist mask has openings that define the interconnect lines;

patterning the first conductive layer in the first region to form first conductive patterns and a bottom plate;

removing the bottom metal resist mask (fig. 20; col. 10, lns.39-59).

12. the interlevel dielectric layer is comprised of oxide formed using a high density plasma enhanced chemical vapor silicon oxide deposition; and interlevel dielectric layer is preferably planarized using a chemical-mechanical polish process (col. 2, lns. 23-43; col. 9, lns. 5-7).

Claims13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al. (6,387,750 B1) in view of Dirnecker et al. (6,646,323 B2).

With respect to claims13 and 14 Lai teaches a method of fabrication of a MIM capacitor comprising the steps of :

providing a semiconductor structure 200 having a first region and a capacitor region;

forming a first conductive layer 202 over the semiconductor structure, wherein the first conductive layer is comprised of A1, Cu and alloys of Al or Cu; and has a thickness in the range of between 3000 and 10,000 A (col.3, lns. 31-32);

patterning the first conductive layer 202 to form a plurality of trenches in the capacitor region, then the trenches extend down into the conductive layer between 24 % and 84 % of the thickness of the first conductive layer (col.3, lns. 35-37);

forming a capacitor dielectric layer 206 over the first conductive layer 202;

patterning the first conductive layer 202 in the first region to form first conductive patterns and a bottom plate.

Reference: figs. 2A-2E with corresponding text.

Lai teaches the features detailed previously but lacks a discussion on the method for:

forming a trench resist layer over the first conductive layer; the trench resist layer has openings that define are as where trenches will be formed in first conductive layer in the capacitor area;

removing the trench resist layer;

forming a top plate over the capacitor dielectric layer in the capacitor region; the top plate is formed by forming a top plate layer over the capacitor dielectric layer, and masking and patterning the top plate layer;

forming an interlevel dielectric layer over the first conductive layer and the top plate;

forming via contacts in the interlevel dielectric layer to contact the top plate, the bottom plate and the first conductive patterns;

forming second conductive layer contacting the via contacts.

However, Dirnecker teaches the method for:

forming a trench resist layer over the first conductive layer; the trench resist layer has openings that define are as where trenches will be formed in first conductive layer in the capacitor area; removing the trench resist layer (col.8, lines 34-52);

forming a top plate 450 or 910 over the capacitor dielectric layer 426 in the capacitor region; the top plate is formed by forming a top plate layer over the capacitor dielectric layer, and masking and patterning the top plate layer (figs.25, 37 with corresponding text);

forming an interlevel dielectric layer 930 over the first conductive layer 910 and the top plate(fig. 37 with corresponding text);

forming via contacts 418 in the interlevel dielectric layer 404 to contact the top plate 450, the bottom plate 424 and 426 and the first conductive patterns 418 (figs.25 with corresponding text);

forming second conductive layer 910 contacting the via contacts 920 (figs. 37 with corresponding text).

Therefore, it would have been obvious to one of ordinary skill in the art to forming MIM capacitor as taught by Lai/ Dirnecker as a means to have a large effective electrode surface area.

Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Dirnecker.

With respect to claims 15-17 Dirnecker teaches a method wherein:

the plurality of trenches formed in a pattern of rows and columns (figs. 28 and 29).

the top plate is formed by forming a top plate layer450 or 910 over the capacitor dielectric layer 426; and masking and patterning the top plate layer (figs.25, 37 with corresponding text);

step (h) further comprises forming a bottom metal resist mask over the first conductive layer; the bottom metal resist mask has openings that define the interconnect lines;

patterning the first conductive layer in the first region to form first conductive patterns and a bottom plate;

removing the bottom metal resist mask (fig. 20; col. 10, lns. 39-59).

Drawings objection

Figure 9, layer "128" should be replace on layer --144--.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor Yevsikov whose telephone number is (571) 272-1910. The examiner can normally be reached on Monday –Thursdays 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, examiner's supervisor, Matthew S. Smith, can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or processing is assigned is (703) 873-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 29, 2004

Victor Yevsikov
Examiner

CARIDAD EVERHART
PRIMARY EXAMINER